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EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,974	GOODE, TERRY LEE	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/20/05*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *04192005*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been presented for examination based on applicant's amendment filed on 12 May 2005. Claims 1-24 remain rejected by the examiner.

Response to Arguments

2. Applicant's arguments filed 12 May 2005 have been fully considered but they are not persuasive in overcoming the prior art rejections.

Regarding applicant's response to drawing objections: Applicant's proposed drawing corrections filed on 12 May 2005 have been approved by the examiner and previous drawing rejections are now withdrawn.

Regarding applicant's response to 103(a) rejections: The examiner first notes that applicant's amendment to the claims has not overcome the existing prior art rejections as proposed in the referenced personal interview of 19 April 2005. The substance of the interview involved an explanation of the operation of the claimed invention that was determined by the examiner to be quite simple. This made it difficult to distinguish any novel features of the invention over the prior art (see interview summary). The examiner had anticipated an amendment to the claims that more precisely defined (i.e. claimed) elements of the claimed invention that would clearly define it over the prior art of record based on the substance of this interview. In a nutshell, applicant's amendment to the claims merely requires a first and second logic device (of any type) configured to emulate first and second circuit partitions. Prior art Boles discloses two functional circuits that are provided with a multiplexer for reconfiguring the input and output pin

signals (Figs. 1-4, Abstract, CL3-L36 to CL4-L4), and first and second pins capable of being configured to provide input or output signals. (CL5-L33-47, Fig. 3). Further, it is well established that programmable logic devices (FPGA's etc.), such those disclosed in the prior art, can be programmed to emulate nearly any circuit configuration and include the ability to reconfigure the device input and output pins. (See: "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment", (Of Record) Babb, Sections 1.1-1.3, 2.2, 3.2, for example) The amended emulator circuit claims of the present invention therefore clearly remain obvious in view of the prior art using the reasoning set forth above and below under 103(a) rejections.

The examiner also notes that applicants appear to engaging in piecemeal analysis of the rejections by arguing, for example, that prior art Sample is directed toward configuring programmable logic arrays and not the use of a serializer and deseralizer. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner therefore maintains the 103(a) rejection of claims 1-24.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. ***Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over EPO Patent application number EP 1 043 662 A1 issued to Boles et al in view of U.S. Patent 6,377,911 issued to Sample et al in further view of U.S. Patent 6,282,503 issued to Okazaki et al.***

Independent claim 1 is drawn to:

emulator circuit on circuit boards comprising:
first/second programmable logic device (PLD)
- first PLD & pins configurable to provide output signals
- second PLD & pins configurable to receive input signals
- serializer coupled to first PLD pins receiving output signals from first PLD & providing serialized data stream;
- cross point switch (CPS) receiving serialized data stream at first CPS input/output pin & routing data stream to second input/output pin of CPS
- de-serializer coupled to second input/output pin of CPS and pins of second PLD receiving data stream from CPS and de-serializing data stream onto pins of second PLD as input signals.

Per independent claim 1: Boles discloses an apparatus and method for configuring the pins (first and second) of two functional circuits (logic devices) to reconfigure input and output pin signals via a multiplexer (Fig. 3). Boles discloses the elements of the claimed limitations of the present invention as follows:

- *first/second programmable logic device (PLD): Boles discloses two functional circuits which are provided with a multiplexer for reconfiguring the input and output pin signals. (Figs. 1-4, Abstract, CL3-L36 to CL4-L4)*

- *first PLD & pins configurable to provide output signals: Boles discloses a first configurable pin capable being configured to provide input or output signals. (CL5-L33-47, Fig. 3)*

- *second PLD & pins configurable to receive input signals: Boles discloses a first configurable pin capable being configured to provide input or output signals. (CL5-L33-47, Fig. 3)*

Boles does not explicitly teach a serializer/de-serializer coupled to first/second PLD input/output pins.

Sample teaches an emulator circuit consisting of multiple programmable logic devices (first, second, etc.) including serial/parallel converters coupled to the input/output of the PLD's for converting data from serial to parallel (de-serializer) and parallel to serial (serializer). (Figs. 7-9, CL8-L62 to CL9-L25) The examiner has interpreted the serial/parallel conversion process of Sample to be functionally equivalent to the serializer/de-serializer of the claimed invention. Sample discloses the elements of the claimed limitations of the present invention as follows:

- serializer coupled to PLD providing serialized data stream: Sample discloses parallel to serial (serializer) and serial to parallel (de-serializer) conversion of data that is input and output from the programmable logic devices (PLD's). (Figs. 7-9, CL8-L62 to CL9-L25)

- de-serializer coupled to input/output of second PLD receiving data stream and de-serializing data stream of PLD as input signals: Sample discloses parallel to serial (serializer) and serial to parallel (de-serializer) conversion of data that is input and output from the programmable logic devices (PLD's). (Figs. 7-9, CL8-L62 to CL9-L25) The examiner also notes that, as recognized by applicants on page 7, line 6 of the specification, the implementation of the serializer/deserializer is known to those skilled in the art and can be easily realized using commercially available IC's such as the S2004 from SMC Corporation (AMCC). Hence, it would have been obvious to a skilled artisan to apply (couple) such devices to the serializing/de-serializing of the input/output data streams to and from the programmable logic devices. (see: AMCC S2004 Device Specification pages 1&2)

Boles and Sample further do not explicitly disclose the use a cross point switch for routing the data stream to input/output pins.

Okazaki discloses a logic emulation system incorporating a cross point switch for routing data stream signals to the input/output pins of a programmable logic device. (Fig. 10, CL6-L19-36). Okazaki discloses the elements of the claimed limitations of the present invention as follows:

- cross point switch (CPS) routing data stream to input/output pins: Okazaki discloses a cross point switch for routing data signals to input and output pins as noted above. (Fig. 10, CL6-L19-36) The examiner again notes that, as recognized by applicants on page 7, line 16 of the specification, the implementation of the cross point switch is known to those skilled in the art and can be easily realized using commercially

available IC's such as the S2016 or S2025 from SMC Corporation. Hence, a skilled artisan would have known to use such devices for routing between the input/output data streams of the first and second programmable logic devices and the cross point switch.

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Boles relating to configuring the pins of functional circuits to provide reconfigured input and output signals via a multiplexer, with the teachings of Sample relating to an emulator circuit consisting of multiple programmable logic devices including serial/parallel converters coupled to the input/output of PLD's for converting serial to parallel (de-serializer) and parallel to serial (serializer) data streams. An obvious motivation exists since, in this case, both Boles and Sample recognize the need for quickly and automatically generating electrically reconfigurable (compatible) hardware with little or no wiring changes for a limited number of device pins (see: Sample CL2-L15-21, Boles CL1-L10-25) Accordingly, a skilled artisan having access to the teachings of Boles and Sample would have knowingly modified the teachings of Boles with the teachings of Sample (or visa versa), to realize the claimed elements of the present invention since the Sample technique (serializing/de-serializing data signals) requires the use of fewer device pins but allows increased data signal flow.

It would have also been obvious to further modify the teachings of Boles with the teachings of Okazaki relating to the use of a cross point switch for routing data signals to the input and output pins since this technique facilitates automatic reconfiguring of the device pins and requires no device wiring changes. (see: Okazaki CL2-L15-30)

Accordingly, a skilled artisan would have been further motivated to modify the teachings of Boles and Sample with the teachings of Okazaki to provide a method for automatic reconfiguring the device pins and routing of the data signals. The level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by each of the references. (See: Boles/Sample/Okazaki, Abstracts) Accordingly, a skilled artisan having access to the teachings of Boles, Sample, and Okazaki would have knowingly modified the teachings of Boles with the teachings of Sample, and further modified the teachings of Boles with the teachings of Okazaki, to realize the claimed elements of the present invention.

Per claim 2: Claim 2 merely requires that the PLD pins be configured to receive the serialized/deserialized data signals and is hence rendered obvious in view of the prior art as cited above. (see: Sample Fig. 8, block 160,, CL8-L62 to CL9-L25)

Per claim 3: Claim 3 includes the additional limitations relating to circuit partitioning (partitioner) and configuring (configurer) the partitions and cross point switch for the first and second circuit elements. In addition to serial/parallel data conversion, Sample also discloses circuit partitioning (partitioner) of netlist interconnections (CL11-L37-67, Figs. 11a-e) and a configuration unit (CL3-L26-31) for configuring (CL11-L43-46) the signal routing based on the partitioning of the circuit elements. Hence, it would have been obvious to further include the partitioning and configuration techniques taught by Sample, with the cross point switch techniques disclosed by Okazki, and the first and second circuit element pin configuring techniques taught by Boles using the same reasoning as previously cited above.

Per claims 4 & 5: Claim 4 includes the element of providing for "virtual interconnections" between elements. This feature is obvious in view of the prior art since all circuit emulators provide a simulated (i.e. "virtual") connection with the emulated target device. (see: Okazaki Background, for example) Claim 5 requires a dedicated signal path to each input/output which is disclosed Boles as noted above. (see: Fig. 2, elements 20 & 22)

Per claims 6 & 7: Claims 6 and 7 require configuring the emulator for static and dynamic operation. Okazaki discloses switching the cross point switch based on logic changes (dynamic) or via the compiler (static) interconnect chip (CL6-L19-33). These limitations are therefore obvious in view of the prior art as noted above.

Regarding independent claim 8: As previously cited above, the combination of Boles, Sample, and Okazaki disclose the of elements cross point switch routing, serializing and de-serializing data streams, and pin configuration of first and second circuit elements. In addition to these limitations, claim 8 includes limitations relating to synthesizing circuit partitions and configuring the circuit partitions and cross point switch routing for the first and second circuit elements. Sample discloses circuit partitioning of netlist interconnections (CL11-L37-67, Figs. 11a-e) and a configuration unit (CL3-L26-31) for configuring (CL11-L43-46) the signal routing based on the partitioning of the circuit elements. Hence, Sample also discloses synthesizing the circuit partitions and method for configuring input/output signals based on the partitions. As also previously cited above, Sample discloses serial/parallel converters coupled to the input/output of PLD's for converting serial to parallel (de-serializer) and parallel to serial (serializer)

data streams (Figs. 7-9, CL8-L62 to CL9-L25). Hence, these limitations are obvious in view of the Boles, Sample, and Okazaki using the same reasoning as cited above.

Per claim 9: Claim 9 merely requires serializing/de-serializing the input/ouput data signals to the PLD's. As cited above, Sample discloses parallel to serial (serializer) and serial to parallel (de-serializer) conversion of data that is input and output from the programmable logic devices (PLD's). (Figs. 7-9, CL8-L62 to CL9-L25) The examiner also notes that, as recognized by applicants on page 7, line 6 of the specification, the implementation of the serializer/deserializer is known to those skilled in the art and can be easily realized using commercially available IC's such as the S2004 from SMC Corporation. Hence, it would have been obvious to a skilled artisan to apply (couple) such devices to the serializing/de-serializing of the input/output data streams to and from the programmable logic devices. (see: AMCC S2004 Device Specification pages 1&2)

Per claims 10 & 11: Claim 10 includes the element of providing for "virtual interconnections" between elements. This feature is obvious in view of the prior art since all circuit emulators provide a simulated (i.e. "virtual") connection with the emulated target device. (see: Okazaki Background, for example) Claim 11 requires a dedicated signal path to each input/output which is disclosed Boles as noted above. (see: Fig. 2, elements 20 & 22)

Per claims 12 & 13: Claims 12 and 13 require configuring the emulator for static and dynamic operation. Okazaki discloses switching the cross point switch based on

logic changes (dynamic) or via the compiler (static) interconnect chip (CL6-L19-33).

These limitations are therefore obvious in view of the prior art as noted above.

Regarding independent claim 14: Independent claim 14 is drawn to:

An emulator circuit comprising:
first/second programmable logic device (PLD)
- first PLD & serializer configurable to receive output signals from user circuit and provide data stream on input/output pin of PLD
- second PLD & de-serializer configurable to receive data stream from input/output pin of PLD
- cross point switch (CPS) receiving serialized data stream at first CPS input/output pin & routing data stream to second input/output pin of CPS

As cited above, Boles discloses an apparatus and method for configuring the pins (first and second) of two functional circuits (logic devices) to reconfigure input and output pin signals via a multiplexer (Fig. 3). Boles discloses the elements of the claimed limitations of the present invention as follows:

- *first/second programmable logic device (PLD): Boles discloses two functional circuits which are provided with a multiplexer for reconfiguring the input and output pin signals. (Figs. 1-4, Abstract, CL3-L36 to CL4-L4)*

- *first PLD & serializer configurable to provide output signals: Boles discloses a first configurable pin capable being configured to provide input or output signals. (CL5-L33-47, Fig. 3)*

- *second PLD & de-serializer configurable to receive input signals: Boles discloses a first configurable pin capable being configured to provide input or output signals. (CL5-L33-47, Fig. 3)*

Boles does not explicitly teach a serializer/de-serializer coupled to first/second PLD input/output pins.

Sample teaches an emulator circuit consisting of multiple programmable logic devices (first, second, etc.) including serial/parallel converters coupled to the input/output of the PLD's for converting data from serial to parallel (de-serializer) and parallel to serial (serializer). (Figs. 7-9, CL8-L62 to CL9-L25) The examiner has interpreted the serial/parallel conversion process of Sample to be functionally equivalent to the serializer/de-serializer of the claimed invention. Sample discloses the elements of the claimed limitations of the present invention as follows:

- serializer configured to provide serialized data stream on PLD input/output: Sample discloses parallel to serial (serializer) and serial to parallel (de-serializer) conversion of data that is input and output from the programmable logic devices (PLD's). (Figs. 7-9, CL8-L62 to CL9-L25)

- de-serializer coupled to input/output of second PLD receiving data stream and de-serializing data stream of PLD as input signals: Sample discloses parallel to serial (serializer) and serial to parallel (de-serializer) conversion of data that is input and output from the programmable logic devices (PLD's). (Figs. 7-9, CL8-L62 to CL9-L25) The examiner also notes that, as recognized by applicants on page 7, line 6 of the specification, the implementation of the serializer/deserializer is known to those skilled in the art and can be easily realized using commercially available IC's such as the S2004 from SMC Corporation. Hence, it would have been obvious to a skilled artisan to apply (couple) such devices to the serializing/de-serializing of the input/output data

streams to and from the programmable logic devices. (see: AMCC S2004 Device Specification pages 1&2)

Boles further does not explicitly disclose the use a cross point switch for routing the data stream to input/output pins.

Okazaki discloses a logic emulation system incorporating a cross point switch for routing data stream signals to the input/output pins of a programmable logic device. (Fig. 10, CL6-L19-36). Okazaki discloses the elements of the claimed limitations of the present invention as follows:

- cross point switch (CPS) routing data stream to input/output pins: Okazaki discloses a cross point switch for routing data signals to input and output pins as noted above. (Fig. 10, CL6-L19-36) The examiner again notes that, as recognized by applicants on page 7, line 16 of the specification, the implementation of the cross point switch is known to those skilled in the art and can be easily realized using commercially available IC's such as the S2016 or S2025 from SMC Corporation. Hence, a skilled artisan would have known to use such devices for routing between the input/output data streams of the first and second programmable logic devices and the cross point switch.

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Boles relating to configuring the pins functional circuits to provide reconfigured input and output signals via a multiplexer, with the teachings of Sample relating to an emulator circuit consisting of multiple programmable logic devices including serial/parallel converters coupled to the input/output of PLD's for converting serial to parallel (de-serializer) and parallel to serial

(serializer) data streams. An obvious motivation exists since, in this case, both Boles and Sample recognize the need for quickly and automatically generating electrically reconfigurable (compatible) hardware with little or no wiring changes for a limited number of device pins (see: Sample CL2-L15-21, Boles CL1-L10-25) Accordingly, a skilled artisan having access to the teachings of Boles and Sample would have knowingly modified the teachings of Boles with the teachings of Sample (or visa versa), to realize the claimed elements of the present invention since the Sample technique (serializing/de-serializing data signals) requires the use of fewer device pins but allows increased data signal flow.

It would have also been obvious to further modify the teachings of Boles with the teachings of Okazaki relating to the use of a cross point switch for routing data signals to the input and output pins since this technique facilitates automatic reconfiguring of the device pins and requires no device wiring changes. (see: Okazaki CL2-L15-30) Accordingly, a skilled artisan would have been further motivated to modify the teachings of Boles and Sample with the teachings of Okazaki to provide a method for automatic reconfiguring the device pins and routing of the data signals. The level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by each of the references. (See: Boles/Sample/Okazaki, Abstracts) Accordingly, a skilled artisan having access to the teachings of Boles, Sample, and Okazaki would have knowingly modified the teachings of Boles with the teachings of Sample, and further modified the teachings of Boles with the teachings of Okazaki, to realize the claimed elements of the present invention.

Per claim 15: Claim 15 includes the additional limitations relating to circuit partitioning (partitioner) and configuring (configurer) the partitions and cross point switch for the first and second circuit elements. In addition to serial/parallel data conversion, Sample also discloses circuit partitioning (partitioner) of netlist interconnections (CL11-L37-67, Figs. 11a-e) and a configuration unit (CL3-L26-31) for configuring (CL11-L43-46) the signal routing based on the partitioning of the circuit elements. Hence, it would have been obvious to further include the partitioning and configuration techniques taught by Sample, with the cross point switch techniques disclosed by Okazki, and the first and second circuit element pin configuring techniques taught by Boles using the same reasoning as previously cited above.

Per claims 16 & 17: Claim 16 includes the element of providing for "virtual interconnections" between elements. This feature is obvious in view of the prior art since all circuit emulators provide a simulated (i.e. "virtual") connection with the emulated target device. (see: Okazaki Background, for example) Claim 17 requires a dedicated signal path to each input/output which is disclosed Boles as noted above. (see: Fig. 2, elements 20 & 22)

Per claims 18 & 19: Claims 18 and 19 require configuring the emulator for static and dynamic operation. Okazaki discloses switching the cross point switch based on logic changes (dynamic) or via the compiler (static) interconnect chip (CL6-L19-33). These limitations are therefore obvious in view of the prior art as noted above.

Per independent claim 20: As previously cited above, the combination of Boles, Sample, and Okazaki disclose the elements of cross point switch routing, serializing and

de-serializing data streams, and pin configuration of first and second circuit elements. In addition to these limitations, claim 20 includes limitations relating to synthesizing circuit partitions and configuring the circuit partitions and cross point switch routing for the first and second circuit elements. Sample discloses circuit partitioning of netlist interconnections (CL11-L37-67, Figs. 11a-e) and a configuration unit (CL3-L26-31) for configuring (CL11-L43-46) the signal routing based on the partitioning of the circuit elements. Hence, Sample also discloses synthesizing the circuit partitions and method for configuring input/output signals based on the partitions. As also previously cited above, Sample discloses serial/parallel converters coupled to the input/output of PLD's for converting serial to parallel (de-serializer) and parallel to serial (serializer) data streams (Figs. 7-9, CL8-L62 to CL9-L25). Hence these limitations are obvious in view of the Boles, Sample, and Okazaki using the same reasoning as cited above.

Per claims 20 & 21: Claim 20 includes the element of providing for "virtual interconnections" between elements. This feature is obvious in view of the prior art since all circuit emulators provide a simulated (i.e. "virtual") connection with the emulated target device. (see: Okazaki Background, for example) Claim 21 requires a dedicated signal path to each input/output which is disclosed Boles as noted above. (see: Fig. 2, elements 20 & 22)

Per claims 23 & 24: Claims 23 and 24 require configuring the emulator for static and dynamic operation. Okazaki discloses switching the cross point switch based on logic changes (dynamic) or via the compiler (static) interconnect chip (CL6-L19-33). These limitations are therefore obvious in view of the prior art as noted above.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,522,985 issued to Swoboda et al teaches emulation modules and emulation adaptors.

U.S. Patent 6,446,249 issued to Wang et al emulation signal routing and partitioning of circuit elements.

"Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators", J. Babb et al, IEEE 0-8166-3890-7/93, IEEE 1993 teaches virtual connections in logic emulators. "Fast Partitioning Method for PLA-Based Architectures", Z. Hasen et al, IEEE 91TH0379-8/91/0000-P2-3.1, IEEE 1991 teaches partitioning in programmable logic devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780.

The Official Fax Numbers are:

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